Power Delivery Design Issues for Hi-Speed USB on Motherboards

Intel Research & Development

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1. Introduction

This document provides guidelines for the proper power delivery design for Hi-Speed USB ports and front panel headers on motherboards. The material covered here is broken up into three main categories: designing for droop test, designing for drop test, and front panel I/O considerations. High speed USB operation is described in the USB Specification Revision 2.0 and USB signal routing on a 4-layer motherboard is described in the High speed USB Platform Design Guidelines, both located at (http://www.usb.org/developers/docs.html).

2. Designing for Voltage Droop

2.1. What is Voltage Droop?

USB allows users to plug and unplug USB devices while the PC is still in operation. When an USB device is plugged into a port, inrush current occur as the newly plugged device's internal bypass capacitor charges to its full potential. This current is drawn from the USB V_{BUS} power plane of the motherboard and causes the V_{BUS} to sag momentarily. This sag is referred to as droop. Voltage droop testing evaluates the port under test's ability to withstand a maximum device equivalent load of 100mA load in parallel with a 10µF capacitor being hot-plugged into an adjacent port. The simulated hot-plug, generated by the droop test fixture, occurs at approximately 1 second interval. The test is conducted with the victim port (port under test) and all other USB ports loaded with 5-unit load (500mA) except the aggressor port (port with the simulated hot-plugging). An oscilloscope is used to monitor the voltage droop amplitude of the V_{BUS} at the victim port. The USB 2.0 specification allows this droop to be no more than 330mV. Figure 1a shows a passing voltage droop signal, while Figure 1b shows a failure in the test.

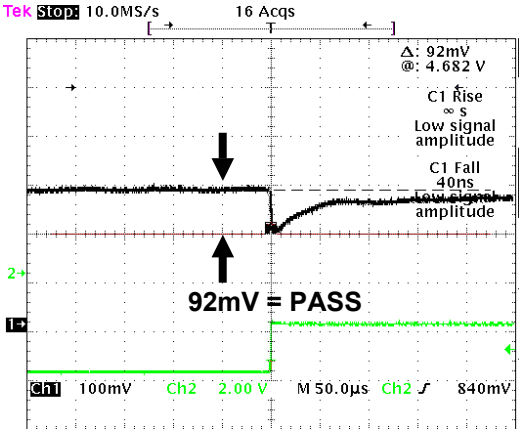


Figure 1a. Voltage droop pass

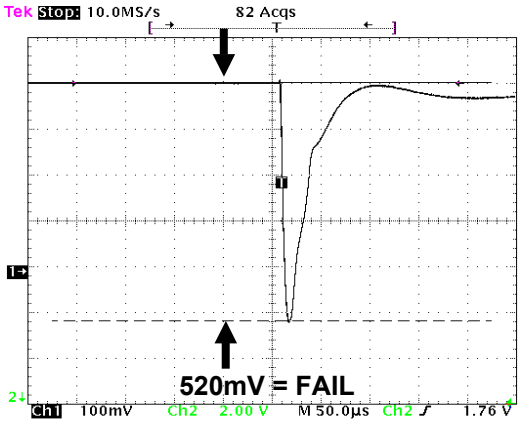


Figure 1b. Voltage droop fail

A majority of droop failures can be attributed to the reasons below:

1. Improper selection of bypass bulk storage capacitor across the V_{BUS} power planes near the USB ports (see section 2.3.1, 2.3.2).
2. Inadequate trace width or poor design of voltage plane between bypass capacitor and USB port (see section 2.3.3).
3. Improper V_{BUS} trace width route from motherboard power supply or voltage regulator to USB port (see section 2.3.3).
4. Improper sizing of fuse element (see section 2.4).
5. Improper placement topology of fuse element (see section 2.4).

2.2. USB Power Line Layout Topology

The following is a suggested topology for power distribution of V_{BUS} to USB ports. Circuits of this type provide two types of protection from inrush current during device hot plugging and unplugging: droop limiting and dynamic detach flyback protection. Dynamic detach flyback occurs when a device that is drawing power from the motherboard is detached causing the inductance in the cable to generate a large flyback voltage.

These two different situations require both bypass capacitance (for droop) and filtering capacitance (for dynamic detach flyback voltage filtering). It is important to minimize the inductance and resistance between the coupling capacitors and the USB ports by making the traces as short and wide as possible.

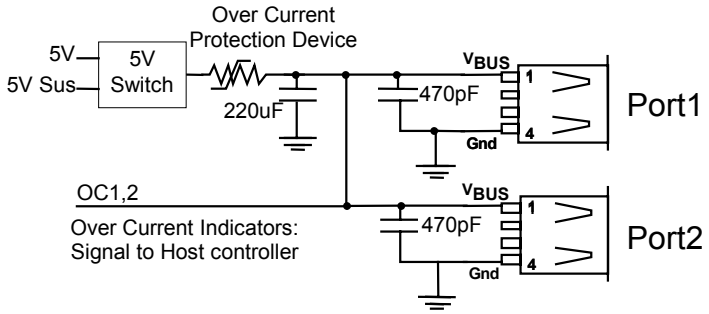


Figure 2. Good downstream power connection (ganged topology)

2.3. Designing to Prevent Voltage Droop

The following recommendations address the most common mistakes made in motherboard design that resulted in droop failure in Hi-Speed USB compliance testing. Although this section doesn't address all the droop issues, it focuses on the most important design guidelines and recommendations that should be followed.

2.3.1. Bypass Bulk Storage Capacitor

It is important to provide sufficient capacitance close to each USB port to prevent the power supplied to the other ports from going out of tolerance. A common mistake that causes voltage droop failure in compliance testing is the selection of the bypass bulk storage capacitor. This capacitor needs to have sufficiently low equivalent series resistance (ESR) in order to function properly. A common problem seen here is the use of inexpensive and low quality bypass bulk storage capacitors that have a high ESR or not enough rated capacitance. In accordance to the USB Specification Revision 2.0, the V_{BUS} power lines must be bypassed with no less than 120µF capacitance of low-ESR capacitance per USB port.

Depending on layout and routing, the designer has the option of using either one or multiple bypass bulk storage capacitors, as long as the total capacitance per port conforms to the above numbers. When replacing multiple bulk storage capacitors with one large one, it is important to be sure to check the proximity of the bypass bulk storage capacitor to the USB port and to use wider traces.

2.3.2. Bypass Capacitor Connection to USB Port

Capacitors should be placed as close as possible to the port and the power-carrying traces should be as wide as possible, preferably, a plane. There should also be double vias on power and ground nets and the trace lengths should be kept as short as possible. Standard bypass routing and design methods should be used at all times to minimize inductance and resistance between bypass bulk storage capacitors and the USB connectors.

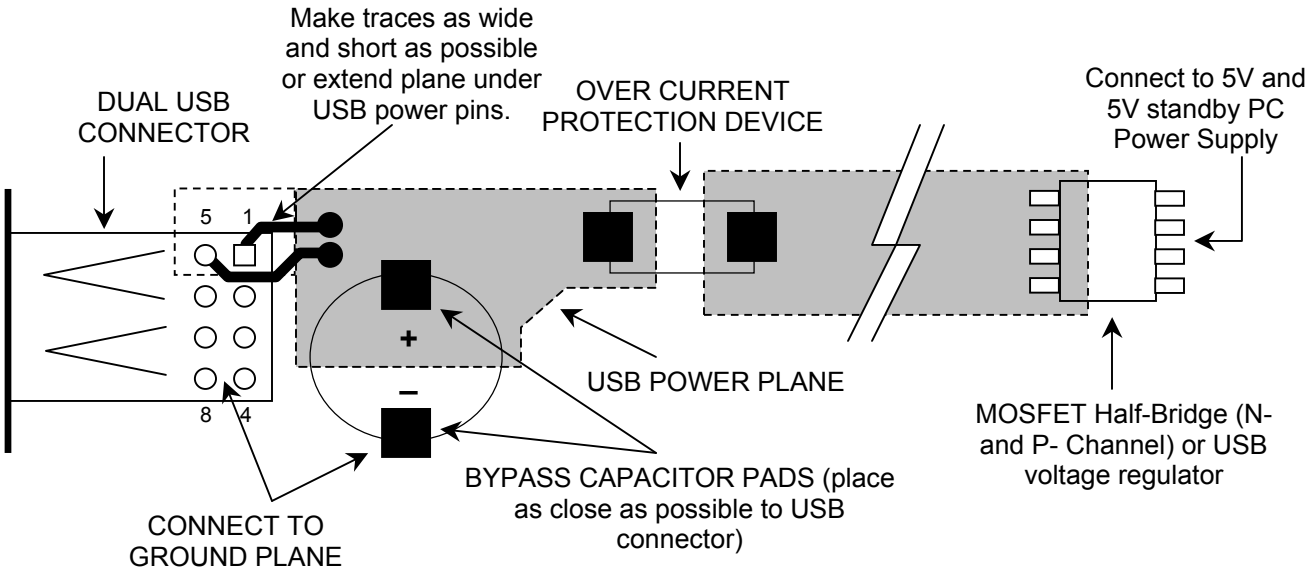


Figure 3. Sample good layout for connections for bypass capacitor, resetable fuse element, and USB connector.

2.3.3. V_{BUS} Trace Width

The trace width for the V_{BUS} current path from the V_{BUS} source to the bypass bulk storage capacitor, over current protection device, and USB connector power and ground pins should be at least 0.050-in.-wide, with 1.5-oz. to 2-oz. copper on outer layer, to ensure adequate current carrying capability.

It is essential to make the power-carrying traces wide enough that the system over current protection will trip instead of fusing the board traces in an overload event. Depending on the rating of the over current protection device, a good "rule of thumb" is to ensure the power-carrying traces are wide enough to carry at least twice the amperage rating of the over current protection device.

Most motherboards use a long route for V_{BUS}, as seen in Figure 4, that must be sufficiently wide in order to support the number of USB ports on the back panel. The power-handling capacity of a printed circuit trace depends mostly on its cross sectional area and the allowable temperature rise.

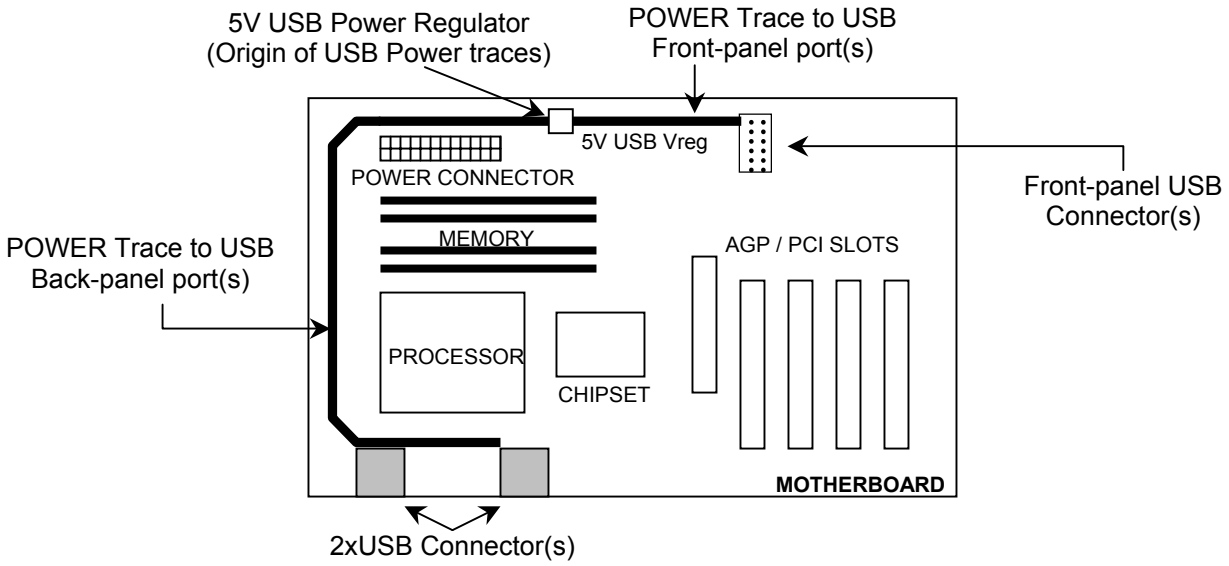


Figure 4. Motherboard placement and common routing for USB power carrying trace.

Figure 5 shows a sample chart relating maximum power-handling capacity to temperatures rise. The horizontal axis measure cross-sectional area in units of square inches for the trace and the vertical axis shows the allowable current for that trace at a given temperature rise. A conservative

upper limit on trace heating inside computing products is 10° C. Such a chart can be used to determine the width of the USB power traces.

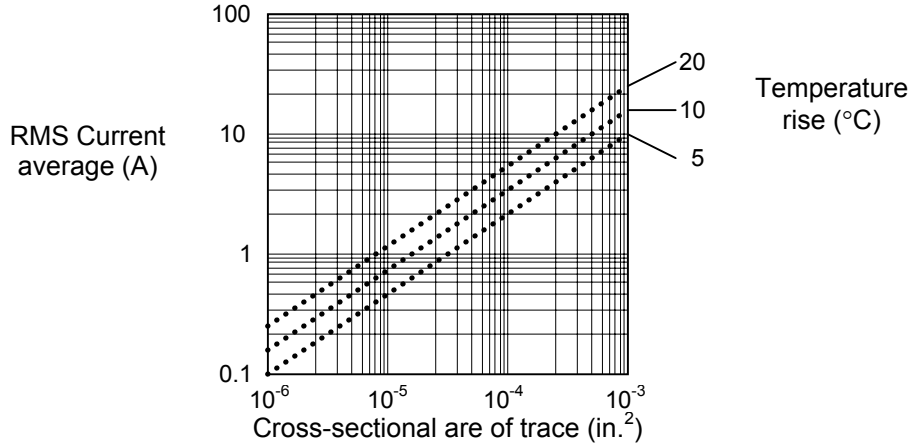


Figure 5. Current-carrying capacity of copper printed circuit traces.
***NOTE: Not actual graph, values used for demonstration purposes only! Check data sheet for accurate values**

As a general rule, wider trace widths are better. However, if your routing channels are restricted, you can achieve the same cross-sectional area by routing two or more power traces using different routes.

2.4. Circuit Protection

For over current protection, USB specification requires that an over current protection device be used in the design of the USB power delivery circuitry. A good motherboard design will have some sort of safety system so as to prevent user, motherboard, and peripheral damage. The purpose of the over current protection device is to limit the amount of current the USB port can draw, such as in a short circuit situation. It should not, however be design to function as a current cop when the downstream device power consumption reaches near the allowable port limits given its declared power requirement. The sizing of the over current protection device should be chosen mainly to protect user safety and against property damage. Over current protection should not be used to enforce the current limits (500mA) that USB devices are required to meet.

2.4.1. Polymeric Positive Temperature Coefficient (PPTC)

PPTC devices (commonly known as polyfuses) are one solution commonly used to meet USB safety requirements. A PPTC device relies on temperature-induced structural changes in a

composite polymer material. The device exhibits low electrical resistance in normal operation and when an over current condition appears, it exhibits a sharply increased resistance. PPTC are popular for use as over current protection devices in USB applications because they are self-resetting and the time-to-trip parameter that PPTCs inherently demonstrate eliminates false circuit trips due to inrush currents. This is the solution of choice for motherboard manufacturers due to price and mentioned operational characteristics.

CAUTION – Please note that as current increases, so does the series resistance of the PPTC, especially if near the maximum current rating. This condition can add unwanted resistance to the circuit.

2.4.2. Port Power Management Device

Port power management devices are typically an integrated circuit design for port power management of USB downstream ports. It provides programmatic control of V_{BUS} power ON and OFF, in addition to over current protection. When current flow exceeds a predefined threshold the silicon device will shut-off the power to the USB port and will assert the USB host controller over current pins OC[5:1]#. For example, if an over current condition occurs on USB port 1, then the power management device for that port will assert OC1 on the USB host controller. These devices are primarily used in USB hubs and rarely found on motherboards due to cost.

When selecting a port power management device, it is important to avoid those that trip when the downstream device slightly exceeds the declared USB power requirement.

2.4.3. Common Mistakes

1. **Selection of over current protection device** – A common mistake that causes compliance failure is under-sizing of the over current protection device. Sizing the over current protection device with too low of a rating will cause droop failure in compliance testing due to added series resistance. It is recommended the preset value be 2.5 to 3 times the maximum allowable port current such that transient currents (e.g., during power up or dynamic attach or reconfiguration) do not trip the over-current protector. The designer should carefully select the fuse device according to average operating current value, operating voltage, ambient temperature, and current-resistance characteristics.

   During initial hot-plug, a legal USB device can draw significant transient current many times above the in-spec operating power consumption. The over current protection device must not limit legal inrush conditions and must tolerate this transient current for about 100 micro-seconds without triggering. This is due to the fact that devices sometimes draw many times the maximum load of 500mA for a brief period of time during hot-plugging. These inrush currents are caused by device initial connections (device capacitance) and transitioning from unconfigured to configured states. A typical in-spec device's inrush

current normally last tens of microseconds and can reach a peak current of a few amperes. Figure 6 shows inrush current event that passes compliance testing.

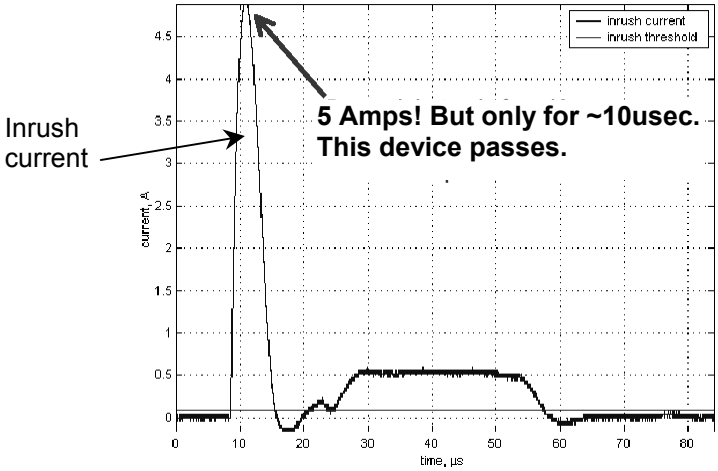


Figure 6. Inrush current for USB device that pass compliance testing.

A conservative approach for protecting multiple ports with a single fuse element is to choose a component with a trip value that is three times the maximum allowable load, as long as it trips before the 5A maximum limit.

For example, if an over current protection device is used to protect for two USB ports, then a reasonable trip level would be 3A or greater. If used for a single port, a reasonable trip value would be 1.5A or greater.

2. **Placement of over current protection device** – Proper placement of over current protection device is also important to avoid droop failure. Figure 7a shows recommended over current protection device placement in a sample circuit. Here the over current protection device is placed upstream (with respect to the power source) of the bypass bulk storage capacitor. Figure 7b shows improper placement of the over current protection device, placed downstream of the bypass bulk storage capacitor. This placement adds additional ESR to the line between the bypass bulk storage capacitor and USB port, mitigating its effectiveness.

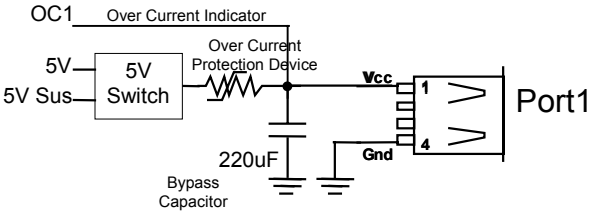


Figure 7a. Correct fuse element layout.

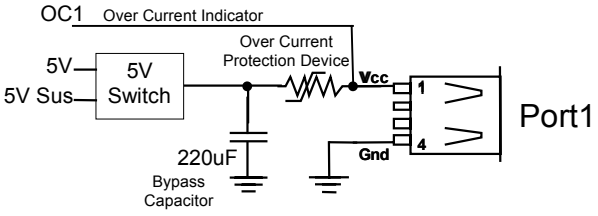


Figure 7b. Incorrect fuse element layout.

It is important to note that individual-port protection offers an advantage over multiple-port (ganged) protection in that if one port fails, the other ports are unaffected. Most cost sensitive designs opt for the ganged topology (see Figure 2).

Please note that some USB host controllers, such as the Intel® I/O Controller Hub with integrated Hi-Speed USB (82801DB ICH4), requires over current reporting to the host controller (input pins OC[5:0]#). These signals set corresponding bits in the USB controllers to indicate that an over current condition has occurred. Please remember to properly connect these over current flags.

3. **Current 'Cops'** – Some port power management device are designed to be current 'cops' in that they will limit if the current draw slightly exceeds the 500mA power consumption limit (the maximum that a USB device is allowed to consume) for high-power bus-powered device. This will cause nuisance trip during hot-plugging of compliant devices. Over current protection devices should not be designed as current 'cops'. Their primary function should be designed to offer safety protection.

3. Designing for Voltage Drop

3.1. What is Voltage Drop?

According to the USB Specification Revision 2.0, the operating voltage of the USB ports must remain in the range of 4.75V to 5.25V while supplying anywhere from 0A to 500mA per port. To ensure all downstream ports meet this requirement, a voltage drop test verifies the voltage between V_{BUS} and GND is within the 4.75V to 5.25V range, when all USB ports in the system are fully (with 500mA load per port) loaded, and also when all USB ports in the system are not loaded.

3.2. Elements Contributing to Voltage Drop

There are some common causes of failures in voltage drop testing:

1. Inadequate power supply rating (see section 3.2.1.)
2. Excessively long system power supply cable harness (see section 3.2.1.).

3. Poor system power supply load regulation (see section 3.2.1.).
4. Underrated over current protection device (see section 3.2.2.).
5. Inadequate Power Trace Width (see section 3.2.3.).
6. Overly resistive ferrite beads (see section 3.2.4.).
7. Inadequate wire gauge for V_{BUS} and GND in the harness of the USB port assembly (see section 3.2.1.).

3.2.1. Inadequate Power Supply or Excessive Length Cable Harness

While budgeting for voltage drop in motherboards, it is important to realize that PC Power supplies often vary in the power delivered to the motherboard. Depending on the vendor's quality control of the PC power supply, the voltage levels delivered to the motherboard can vary (V_{NL}=4.95V, V_{NL}=5.1V, etc.) from vendor to vendor, as well as on a per unit basis.

It is important to note that using a PC power supply that minimally meets the *ATX/ATX12V Power Supply Design Guide* is insufficient to pass USB requirements. According to the ATX specification, the DC output voltages shall remain within the regulation ranges of 5V ±5% (4.75V to 5.25V) when measured at the load end of the output connectors under all line, load, and environmental conditions. This is insufficient to pass USB requirements since a power supply operating on the lower voltage range will have zero budget left for motherboard routing and component voltage drop. It has been known for motherboards to have upwards of 350mV of voltage drop, thus requiring minimum 5.15V power supply in order to pass USB electrical test. Please select power supplies carefully so they provide sufficient voltage for system/motherboard in order to pass USB electrical test.

PC power supply wire harnesses also add voltage drop due to the resistance associated with the connecting wires and can add considerable resistance if wire harness length is excessive. Note that there are no specific requirements for output wire harness lengths. Ideally, wires should be short to minimize electrical impedance and it is recommended they be at least 18AWG (16AWG for 300W configurations).

3.2.2. Underrated Over Current Protection Device

As with droop testing, the use of an underrated fuse element can cause voltage drop failure. An underrated fuse element is likely to have a higher than desired resistance, thus adding excessive voltage drop across the component. The commonly used PPTC in motherboards exhibits exponential increase in resistance with increase over ambient temperature, thus resulting in increased voltage drop. Improper sizing here can result in USB compliance failure.

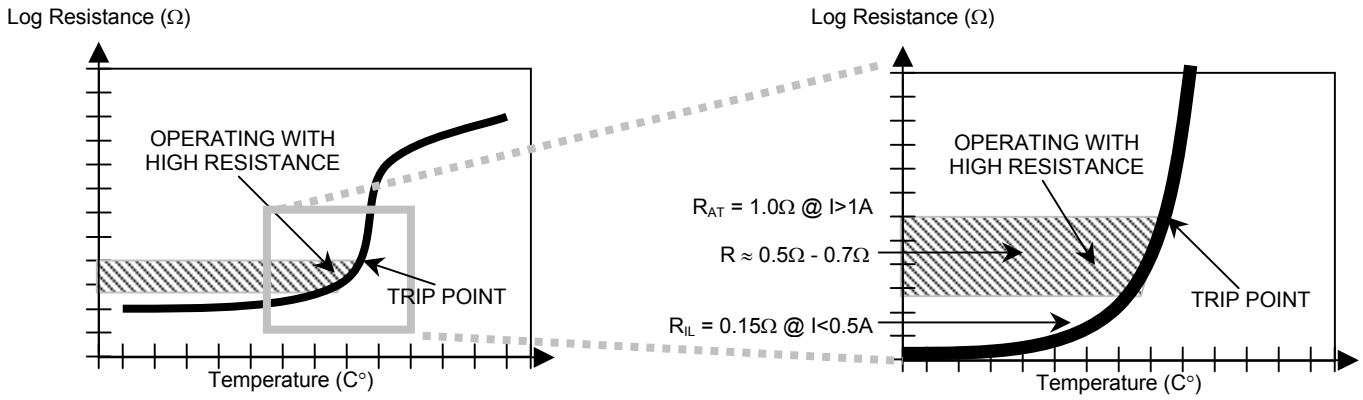


Figure 8. Graph of PPTC performance with increasing heat caused by overcurrent.
***NOTE: Not actual graph, values used for demonstration purposes only! Check data sheet for accurate values.**

Figure 8 shows a sample operation of a surface mount PPTC rated at hold current (I_{HOLD}) of 0.50A and trip current (I_{TRIP}) of 1.00A. The resistance before trip time is in the range between 0.5Ω and 1.0Ω, significantly higher than its resistance at normal operating current (R_{IL}), rated at 0.15Ω. Calculations below show how operation with high resistance will cause drop failure.

$$V_{DROP} = I_{LOAD} \times R_{FUSE}$$

$V_{DROP\_FUSE} = 500mA \times 0.15\Omega = 0.15V$

$V_{NL} = 5.0V$ **(PC Power Supply)**

$V_{LOAD} = V_{NL} - V_{DROP\_FUSE}$

$V_{LOAD} = 5V - 0.15V = 4.85V$

PASSES USB-IF Voltage Drop Test and has additional 0.10V for additional voltage drop budgeting.

$V_{DROP\_FUSE} = 500mA \times 0.7\Omega = 0.35V$

$V_{NL} = 5.0V$ **(PC Power Supply)**

$V_{LOAD} = V_{NL} - V_{DROP\_FUSE}$

$V_{LOAD} = 5.0V - 0.35V = 4.65V$

FAILS USB-IF Voltage Drop Test.

By selecting a higher rated resetable fuse element, the designer can further reduce fuse element resistance (R_{IL}). This will allow for better voltage drop budgeting. Below table shows some sample values for a surface mount PTC.

I_{HOLD} (A)	I_{TRIP} (A)	R_{IL} (Ω)
0.50*	1.00*	0.15*
0.75*	1.50*	0.11*
1.10*	2.20*	0.04*
1.25*	2.50*	0.035*
1.50*	3.00*	0.030*

Table 1. Sample operating values for surface mount resetable fuse element.
***NOTE: Not actual table, values used for demonstration purposes only! Check data sheet of your device for specific values.**

3.2.3. Inadequate Power Trace Width

The most common cause of voltage drop failure in USB power delivery is the resistance associated with the V_{BUS} trace. While budgeting for voltage drop, the designer must take into account the trace length, maximum current being supplied for normal operation, and total resistance associated with the V_{BUS} trace. There are many tools out on the web that can perform trace width, length, and total resistance calculations.

For example, a power carrying trace that supplies 3A, at a distance of 20-inches, 0.100-in.-wide, with 2-oz. copper on outer layer will have a total resistance of approx. 0.046Ω and voltage drop of 0.14V. The same trace at 0.050-in.-wide will have a total resistance of approx. 0.09Ω and voltage drop of 0.28V. Make power traces as wide as possible!

3.2.4. Overly Resistive Ferrite Beads

Ferrite beads (or ferrite chokes) are sometimes used in the current path of motherboards to meet EMI (Electro-Magnetic Interference) requirements. Improper selection of ferrite beads can cause voltage drop failure. Depending on dimensions and rating, ferrite beads can exhibit high DC resistances (DCR) at maximum current rating. For example, a ferrite bead in 1206 packaging with max. current rating of 1000mA will have 0.1Ω resistance. This will result in a voltage drop of 0.1V.

Ferrite beads are nominally placed between the bypass capacitor and the USB port pin on V_{BUS}.

3.3. Voltage Drop Budgeting

Voltage drop budgeting is an important task to take into account when designing for the power delivery to the USB ports. Figure 9 shows all the areas that will contribute to voltage drop on the USB port of a motherboard. By determining approximate IR drop associated with the wire harness, resetable fuse element, the allowable operating voltage range of the PC power supply, then the designer will have some left over IR drop to determine the minimum width of the V_{BUS} trace to meet the 4.75V minimum and 5.25V maximum requirements (Equation 1).

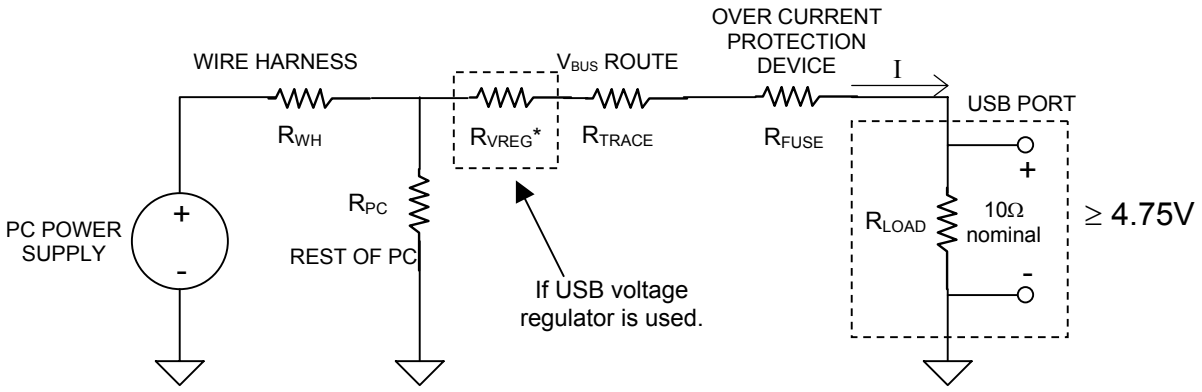


Figure 9. Areas that contribute voltage drop for USB port on a motherboard.

Equation 1 – Voltage Drop Budgeting

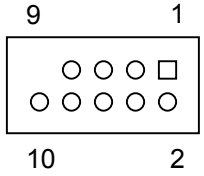
$$5.25V \geq V_{PC\_POWER\_SUPPLY} - [\,(I \times R_{WIRE\_HARNESS}) + (I \times R_{VBUS\_TRACE}) + (I \times R_{V\ REG}) + (I \times R_{FUSE\ ELEMENT})\,] \geq 4.75V$$

4. Front Panel Design Considerations

Many motherboards include support for USB ports that are not located on the motherboard (e.g. front panel connectors). This support is typically provided by stake pins on the motherboard with a cable going to the front panel connectors. Some cables have integrated USB connectors at the end of them, other solutions have a separate front panel daughter card where the USB connectors are mounted. The following section provides guidelines to ensure quality front panel header design for different front panel solutions.

4.1. Front Panel USB Header Design and Pin-out

A ten pin, 0.1-inch stake pin assembly is recommended. Each 2x5 header supports two ports. Figure 10 shows a sample Front Panel USB header and description of pin outs.



Pin	Signal Name	Description
1	VREG_FP_USBPWR0	Front Panel USB Power (Ports 0,1)
2	VREG_FP_USBPWR0	Front Panel USB Power (Ports 0,1)
3	USB_FP_P0-	Front Panel USB Port 0 Negative Signal
4	USB_FP_P1-	Front Panel USB Port 1 Negative Signal
5	USB_FP_P0+	Front Panel USB Port 0 Positive Signal
6	USB_FP_P1+	Front Panel USB Port 1 Positive Signal
7	Ground	
8	Ground	
9	KEY	
10	USB_FP_OC	Front Panel USB Overcurrent signal (Ports 0,1) *(OPTIONAL – used if fuse element is provided on front panel daughterboard)*

Figure 10 – Front panel USB header pin-out

4.2. Front Panel Header Routing and Component Placement

It is recommended that the over current protection device for the front panel header be included on the motherboard to prevent damage to the motherboard. This should be implemented only if the front panel solution does not include a connector card that includes over current protection. If a specific front panel cable solution is not provided, it is safer to assume the front panel solution won't provide over current protection. With this being the case, include the over current protection on the board and clearly document that over current protection is provided on the board. Be sure to place the over current protection device downstream of the bypass bulk storage capacitor so not to cause droop failure.

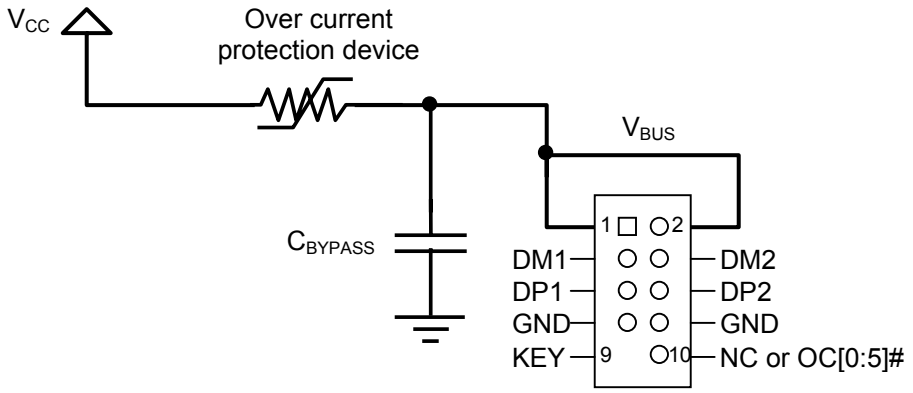


Figure 11 – Front panel USB header schematic

The location of the Front Panel I/O header on the motherboard should take into account the trace lengths on the motherboard and interface board as well as the front panel cable length; otherwise signal quality could be affected. See the USB Specification Revision 2.0 and the Front Panel I/O Connectivity Design Guide for details and testing information.

When performing routing to the USB front panel connector pins, please follow these routing considerations:

1. Traces or surface shapes from VCC to the over current protection device, to C_{BYPASS} and to the connector power and ground pins should be at least 50 mils wide to ensure adequate current carrying capability.
2. There should be double vias on power and ground nets, and the trace lengths should be kept as short as possible.

4.3. Cable and Connector Card

There are two options in designing for front panel USB connectors: the use of a front panel combined cable and connector solution and the use of a daughter card or connector card, as seen in Figures 12a and 12b.

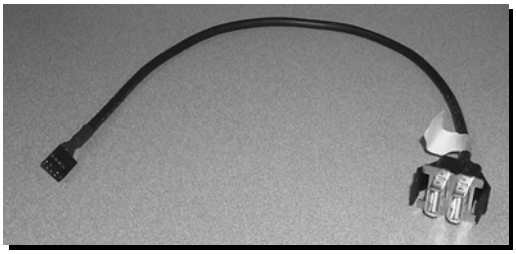


Figure 12a. Combined cable and connector solution.

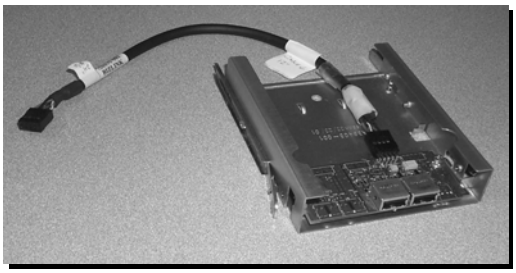


Figure 12b. Connector card with cabling.

When designing for the combined front panel cable/connector solution, the EMI/ESD/fuse components need to be placed on the motherboard close to the front panel header. Rules in Section 4.2 apply in the routing and component placement.

On the other hand, if the system integrator plans to use a connector card, it is important not to have duplicate EMI/ESD/fuse components placed on the motherboard, as this will usually cause drop/droop and signal quality degradation or failure. In connector card design, please follow the following guidelines:

1. Place the V_{BUS} bypass bulk storage capacitance and ESD suppression components on the connector card as close as possible to the connector pins.
2. Follow the same layout, routing and impedance control guidelines as specified for motherboards.
3. Minimize the trace length on the front panel connector card. Less than 1-inch trace length is recommended.
4. Use the same mating connector pin-out as outlined for the motherboard in Section 4.1.

4.4. Front Panel Cabling

When designing for a front panel USB interface cable to be used in conjunction with the front panel I/O interface board and main board, it is important to follow proper cable specifications. The requirements are listed in Section 4.4 of the Front Panel I/O Connectivity Design Guide. Both cable length and cables with an impedance variation outside of the USB Specification limits could cause front panel USB devices to fail to operate reliably. Please refer to above design guide for proper cable selection.

5. Conclusion

This paper is intended as a guide in designing power delivery for USB ports on motherboards. The paper addresses the most common issues causing USB-IF electrical test failures and design methods to prevent such problems.

For motherboard and system compliance testing, please contact one of the Independent Test Labs. For the latest information on USB-IF Compliance testing and test requirements, please visit the USB-IF Compliance Program web site.

Here are additional guides that can be useful in designing for USB:

- ***Universal Serial Bus Revision 2.0 Specification*** – http://www.usb.org/developers/data/usb_20.zip
- ***High Speed USB Platform Design Guidelines*** – http://www.usb.org/developers/data/hs_usb_pdg_r1_0.pdf
- ***Front Panel I/O Connectivity Design Guide*** – http://www.formfactors.org/developer/fpio_design_guideline.pdf .
- ***ATX/ATX12V Power Supply Design Guide*** – http://www.formfactors.org/developer/specs/atx/atx12vPSDGV1.pdf .
- ***USB-IF USB 2.0 Electrical Test Specification*** – http://www.usb.org/developers/data/compliance/USB-IF_USB_2.0_Electrical_Test_Spec.pdf

If you have further questions or comments regarding areas discussed in this paper, please send all correspondence to admin@usb.org.